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Vertical Semiconductor Nanowires on Metal Substrate

Technology ID
20160145

Category
Engineering & Physical Sciences/Instrumentation, Sensors & Controls
Engineering & Physical Sciences/Materials
Engineering & Physical Sciences/Nanotechnology
Engineering & Physical Sciences/Semiconductor

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Photoresist and Etching Fabrication Method

Vertically oriented semiconductor nanowires are created on a metal substrate by a fabrication method that combines photoresist and etching. The simplified photolithography process simplifies nanowire creation and improves precision/control of nanowire density by forming high aspect ratio porous structures with improved side wall quality and high yield. After a developer creates resist patterns, an aluminum layer is etched in regions (patterns) of varying thickness before anodization. This allows nanoporous structures to form on the patterned region at early stages of anodization and grow semiconductor and metal nanowires through the nanopore template so that vertically aligned nanowire arrays or single nanowires with metal or semiconductor materials are realized at the desired areas on metal surface. This new approach does not require a metal oxide mask layer to protect the aluminum layer before an anodization process, and does not require that nanopores be covered before metal nanowire growth.

MN-IP Try and Buy

Try

- Trial period is up to 12 months
- Trial fee is $5000/6 months
- Trial fee is waived for MN companies or if sponsoring $50,000+ research with the University
- No US patent expenses during trial period

Buy

- $25,000 conversion fee (TRY to BUY)
- Royalty rate of 3% (2% for MN company)
- Royalty free for first $1M in sales

Simplified Photolithography Process

Fabricating vertically aligned nanowires is typically done on silicon substrate, while comparable devices on a metal substrate require a complex and expensive chemical vapor deposition process impractical for large area devices. This technology simplifies the process, potentially lowers costs and results in higher yields.

BENEFITS AND FEATURES:

- Very regular or irregular distribution of vertically aligned semiconductor or metal nanowires on a metal substrate
- High aspect ratio nanowires
- High yield: close to 100%
- 50 nm x 1um aspect ratio
- Cost effective: requires no metal oxide mask layer; no need to cover nanopores

APPLICATIONS:

- Biological, chemical and nanowire based sensors
- Photovoltaic cells
- 3D transistors
- LED lighting; organic LED performance
- Field electron devices
- Next generation computer memory (phase change memory)
- Semiconductor nanowire solar cell devices

Phase of Development - Prototype: lab has fabricated vertically aligned metal (gold) and semiconductor (silicon) nanowires on metal (platinum) substrate with 50 nm x 1um aspect ratio.

Researchers

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Publications

Patterning Anodic Porous Alumina with Resist Developers for Patterned Nanowire Formation
Material Research Society Online Proceedings Library Archive, Volume 1785 January 2015, pp. 13-18