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Ultra High Density Integrated Composite Capacitor Design for CMOS

Technology No. 20160011

IP Status: Issued US Patent; **Application #:** 15/132,326

High Capacitance, Low Leakage, Requires Less Chip Area

An ultra-high density two-terminal integrated composite capacitor uses a parallel combination of metal oxide metal (MOM), metal oxide silicon (MOS) and metal insulator metal (MIM) capacitors physically laid over one another. This design both conserves area while providing capacitance density comparable to deep trench capacitors. The MOS capacitor, used in accumulation mode, offers high capacitance and low leakage. Floating the MOS source and drain terminals significantly reduces overall system leakage. This capacitor can be used in general-purpose, mixed-signal blocks as well as regular CMOS processes.

MN-IP Try and Buy

Try

- Trial period is up to 12 months
- Trial fee is $5,000 for twelve months
- Trial fee is wavied for MN companies or if sponsoring $50,000+ research with the University
- No US patent expenses during trial period

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- $10,000 conversion fee (TRY to BUY)
- Royalty rate of 3% (2% for MN company)
- Royalty free for first $1M in sales

More Effective than Deep Trench Capacitors

Custom-fabricated deep trench capacitors are expensive and not available in regular, mixed-signal fabrication processes. This ultra-dense capacitor offers a more cost effective alternative to such specialized and expensive integrated capacitors while producing comparable capacitance density. In addition, it saves active chip area (8X) in regular CMOS process and reduces leakage wastage by 40 times.

BENEFITS AND FEATURES:

- Devices benefit from ultra high density
- Three capacitors stacked one over another
- MOM (Metal Oxide Metal), MOS (Metal Oxide Silicon) and MIM (Metal Insulator Metal) capacitors
- Power loss leakage decreased by 40X
- Saves active chip area by eight (8) times
- Floating MOS capacitor source and drain

APPLICATIONS:

- General-purpose, mixed signal blocks
- CMOS processes
- Switched capacitor DC-DC converters
- Switched capacitor amplifiers in ADCs
- Power converters

Phase of Development - a capacitor was fabricated in a 65nm CMOS process

Researchers

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Publications

Fully tunable software defined DC-DC converter with 3000X output current & 4X output voltage ranges
IEEE Xplore 2017, 27 July 2017

Interested in Licensing?

The University relies on industry partners to further develop and ultimately commercialize this technology. The license is for the sale, manufacture or use of products claimed by the patents. Please contact us to share your business needs and licensing and technical interests in this technology.

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