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Ultra Broadband Coplanar Waveguide Through Silicon Via Transition (20110024, Dr. Rhonda Franklin)

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Engineering & Physical Sciences/Semiconductor

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Through Silicon Via For 3D Semiconductor Packaging

In recent years, semiconductor manufacturers have shifted toward 3D packaging. The interconnect length between dies in a microchip impacts clock speed, power dissipation and integration density. By moving from a 2D configuration to a 3D configuration, the interconnect length can be reduced, which can increase clock rates, lower power dissipation, and increase integration density. A leading interconnect candidate for 3D packaging is the Through Silicon Via (TSV), but currently suffers from insufficient bandwidth.

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Ultra Broadband Coplanar Waveguide TSV Technology

The University of Minnesota interconnect technology is an ultra broadband coplanar waveguide (CPW) TSV that operates from DC to 110 GHz with high return loss and low insertion loss. Truncation of the ground plane and use of air trenches enable superior TSV performance but occupy minimal real estate on the chip. The resulting bandwidth is much broader than conventional TSVs and enables higher performance and decreased power consumption for applications that require ultra broadband performance. The technology is compatible with current semiconductor practices and is expected to be low-cost. This technology has applications in 3D interconnect chip packaging for CMOS image sensors, memory stacks, logic stacks, and field-programmable gate arrays.

FEATURES AND BENEFITS OF ULTRA BROADBAND COPLANAR WAVEGUIDE TSV:

- Increased broadband performance - up to 110 GHz
- Has high return loss and low insertion loss
- Compact design
- 80% improvement in bandwidth compared to conventional TSV
- Low cost – compatible with current semiconductor practices

Researchers

Rhonda Franklin, PhD

Associate Professor, Department of Electrical and Computer Engineering, College of Science and Engineering

External Link (www.ece.umn.edu)