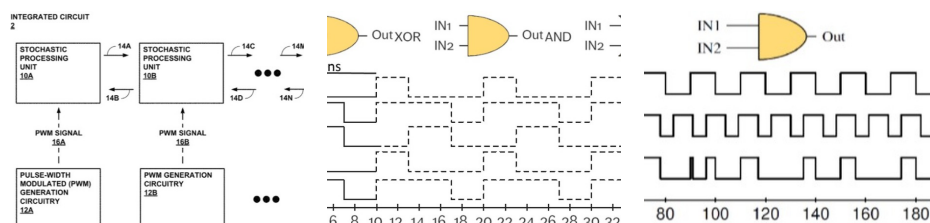




Stochastic computing on pulse-width modulated signals

A low-cost system for computing stochastically using periodic analog signals.



IP Status: US Patent Issued; **Application #:** 15/869,453

Applications

- Stochastic computing - image/signal processing, neural networks

Key Benefits & Differentiators

- A new, energy-efficient, high-performance, and much less costly approach for Stochastic Computation
- Able to carry out a range of stochastic operations using time-encoded data
- Operations with independent inputs (multiplication, scaled addition) using inharmonic PWM signals
- Operations with correlated inputs (subtraction, min, max, comparison) using synchronous PWM signals
- An excellent fit for low-power applications that include time-based sensors (e.g., vision chips)
- Compared to currently available technologies
 - 99% performance speedup
 - 98% saving in energy consumption
 - 40% area reduction

Overview

In stochastic computing, circuits operate on randomized bit streams. Currently, physical random sources or pseudo-random constructs such as linear-feedback shift registers (LFSRs) are used to generate random bit streams. However, these stochastic number generators can account for as much as 80% of the total stochastic circuit cost. Additionally, long run-time of stochastic circuits, together with the high power consumption of the existing stochastic number generators, could lead to significantly higher energy use than their conventional binary counterparts.

Researchers at the University of Minnesota have developed a novel system for generating stochastic bit streams using analog periodic pulse signals. Exploiting pulse width modulation (PWM), signals corresponding to specific values are generated by adjusting the frequency and

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Category

Engineering & Physical
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duty cycles of PWM signals. With this approach, the latency, area and energy consumption are all greatly reduced. Experimental results show up to 99% performance speedup, 98% saving in energy consumption, and 40% area reduction compared to existing methods.

In this technology, instead of communicating data to and from the stochastic computation components in the form of random or pseudo-random digital stochastic bit streams, the bit streams are communicated as pulse-width modulated signals. Signal generators can be configured to generate and output the signals, for example, by adjusting the frequency (periods) and duty cycles so as to encode values in a manner that allows the encoded analog signals to be utilized with conventional stochastic digital logic components. The approach is motivated by the observation that, as technology has scaled and device sizes have gotten smaller, the supply voltages have dropped while the device speeds have improved. Control of the dynamic range in the voltage domain is limited; however, control of the length of pulses in the time domain can be precise. Encoding data in the time domain may be more accurate and more efficient than converting signals into binary radix. The transformative idea in this invention is a technique for performing computation on time-encoded analog values directly with ordinary CMOS digital logic. This technology is suitable for applications in digital or analog chips operating in domains such as image processing and signal processing in general. This technology could also be applied to approximate computing applications and operations that tolerate some degree of uncertainty (such as video processing, image tagging).

Phase of Development

TRL: 2-3

Theoretical foundation has been developed. Circuit simulations have validated the concept.

Desired Partnerships

This technology is now available for:

- License
- Sponsored research
- Co-development

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References

1. Najafi, M. H., Jamali-Zavareh, S., Lilja, D. J., Riedel, M. D., Bazargan, K., & Harjani, R. , <https://doi.org/10.1109/TVLSI.2016.2645902>, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 25(5), 1644-1657.
2. Najafi, M. H., & Lilja, D. J. , <https://doi.org/10.1109/ASPAC.2017.7858369>, In 2017 22nd Asia and South Pacific Design Automation Conference (ASP-DAC) (pp. 481-487). IEEE.
3. Najafi, M. H., Jamali-Zavareh, S., Lilja, D. J., Riedel, M. D., Bazargan, K., & Harjani, R. , <https://doi.org/10.1109/MM.2017.4241345>, IEEE Micro (2017), 37(6), 62-71.