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Optimizing Processors for IoT Applications

Chip design component and path optimization

This technology is a portfolio of methods for optimizing circuit and chip design to obtain processors that are smaller, less complex and consume less power than their full featured counterparts.

- Characterize circuit paths to identify the highest activity, longest exercised path and worst exercised path in terms of timing slack, number of toggles and timing slack range.
- Generate application-specific processors from general purpose processors by identifying the components that will not exercise, eliminate those components and further optimizes the design.

These novel, dynamic techniques are designed around gate-based, rather than path-based analysis, which recognizes that a set of gates maps to a unique set of paths in a design. Gate-based analysis can efficiently analyze large designs over large time windows, even full processor designs and full applications.

Efficiently characterizes paths

Current techniques enumerate a circuit's paths to identify the longest exercised and highest activity paths. This enumeration is not scalable, due to the large number of paths in modern digital designs. This new method efficiently captures in a gate level simulation the set of paths activated by an application. This information can be used for targeted processor optimizations.

Enhances battery life of simple devices

Processors that run simple programs (e.g., for door/window sensors, remote sensors, IoT (internet of things) devices, heart rate monitors, etc.) require extended battery life. Demand for simple processors are growing as current devices use full featured, general-purpose processors that incur higher power and area overheads. This new automated approach generates application-specific processors that reduce the area and power requirements of the chip. The technology analyzes the software and the chip's CAD file to identify portions of the processors that can be turned off or removed, thus enhancing the battery life.

Phase of Development

- Prototype developed.

Benefits

- Smaller footprint
- Lower power requirements, longer battery life
- Optimized processor design

Features

Technology ID

20170333

Category

Engineering & Physical Sciences/Design Specifications
Engineering & Physical Sciences/Semiconductor
Software & IT/Algorithms

Learn more

- Efficiently captures exercised paths of a gate level simulation
- Reports worst exercised paths (i.e., timing slack, activity, and within timing slack range)
- Optimizes design for various metrics (e.g., delay and power)
- Identifies processor components that an application will not exercise and eliminates those components
- Automatically generates application-specific processors from general purpose processors

Applications

- Chip / processor design
- Tools for processor performance
- Processor optimization

Researchers

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Publications

Bespoke Processors for Applications with Ultra-low Area and Power Constraints
IEEE Micro, Volume 38, Issue 3, May-June 2018, Pages 32-39

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