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Hybrid charge trap transistor-MRAM memory devices (2020-102, Dr. Jian-Ping Wang)

Designs of hybrid charge trap transistor-MRAM devices for ultra-high-density non-volatile memory.

IP Status: US Patent Issued # 11,328,757

Applications

- Non-volatile memory in electronic devices

Key Benefits & Differentiators

- Usage of flash and MRAM components facilitates
    - write operations independent for one another
    - 2 data bit storage per memory cell
    - high storage density, low power consumption
- Usage of polycrystalline BiSe makes the designs **suitable for CMOS fabrication process**

Integrated flash and MRAM device

Prof. Wang's group at the University of Minnesota has recently demonstrated that sputtered topological insulator field effect transistors (FETs) can be used as charge trap devices. The unique charge-to-spin conversion of topological insulator introduces an opportunity to be integrated with ferromagnets to create hybrid charge trap transistor-Magnetoresistive random-access memory (MRAM) devices. Such hybrid devices, **capable of storing 2 data bits in each memory cell** - one data bit in the charge trap layer (flash) and another data bit in the ferromagnetic layer (MRAM), paves the way to the development of novel ultra-high-density non-volatile memory.

Four different device designs are conceptualized based on the basic principle of integrating a topological insulator-based charge trap transistor with an MRAM component. Each of these designs present non-trivial 4-state storage, with unique writing and reading techniques (SOT, STT, VCEC) based on their specific operation, stack design, and transport physics. Some of these designs utilize in-plane or perpendicular Magnetic Tunneling Junctions to optimize the read-write operation. These integrated designs boasts advantageous attributes of both flash and MRAM technologies while maintaining **CMOS-friendly manufacturing process.**

Phase of Development

The charge trap devices has been demonstrated experimentally. The charge trap-MRAM integrated devices are proposed for the first time.

Researchers

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Technology ID

2020-102

Category

Engineering & Physical Sciences/Design Specifications
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