



Electromigration on Signal Interconnects (20140089, Dr. Sachin Sapatnekar)

Technology ID

20140089

Category

Engineering & Physical
Sciences/Nanotechnology
Engineering & Physical
Sciences/Semiconductor
Software & IT/Algorithms
Software & IT/Simulation &
Modeling

Efficiently Characterizes Cell-internal Electromigration

The problem of cell-internal electromigration (EM) on signal interconnects within a standard cell is solved using this technology which efficiently characterizes EM characteristics of gates in a standard cell library, under all pin positions, based on a single circuit simulation and graph-based methods. The approach uses Joule heating effects to model and efficiently characterize cell-internal EM to analyze the lifetime of large benchmark circuits. A related method optimizes circuit lifetime by changing pin positions in gates within a circuit. This procedure has demonstrated an approximate 60% increase in circuit lifetime.

Optimization of Circuit Lifetime

Standard cell-based gate libraries are the bedrock of integrated circuit design. Electromigration (EM) in on-chip metal interconnects is a critical reliability failure mechanism in nanometer-scale technologies and is an increasing problem in integrated circuits that reduces circuit lifetime. Traditionally, EM affected global wires, but in current and future technologies, within-gate wires will also be significantly affected. Currently, EM checks in existing technologies are performed ad hoc; no current methods systematically perform cell-internal EM or allocate pin positions to increase the lifetime of a circuit that uses numerous standard cells. This technology provides a systematic and computationally efficient way for analyzing cell-level EM and translating it to an analysis and optimization of circuit level lifetimes.

BENEFITS AND FEATURES:

- Models and efficiently characterizes cell-internal EM
- Characterizes EM characteristics of gates in a standard cell library under all pin positions
- Analyzes lifetime of large benchmark circuits
- Optimizes circuit lifetime
- Joule heating effects
- Solves cell-internal EM problems
- Approximate 60% increase in circuit lifetime

APPLICATIONS:

- Integrated circuit design
- Circuit design

Phase of Development - Prototype dev

Researchers

Sachin Sapatnekar, PhD

Professor, Electrical and Computer Engineering, University of Minnesota

[External Link](http://ece.umn.edu) (ece.umn.edu)

Vivek Mishra, PhD

Electrical and Computer Engineering, University of Minnesota

Palkesh Jain, PhD

Ricardo Reis, PhD

Learn more



Universidade Federal do Rio Grande do Sul , Brazil

Gracieli Posser, PhD

Universidade Federal do Rio Grande do Sul , Brazil

Publications

[*A Systematic Approach for Analyzing and Optimizing Cell-Internal Signal Electromigration*](#)

IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, ICCAD. 2015, pp. 486 – 491, 2014

[*Cell-Internal Electromigration: Analysis and Pin Placement Based Optimization*](#)

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 35, No. 2, pp. 220 – 231, February 2016

Interested in Licensing?

The University relies on industry partners to scale up technologies to large enough production capacity for commercial purposes. The license is available for this technology and would be for the sale, manufacture or use of products claimed by the issued patents. Please contact us to share your business needs and technical interest in this technology and if you are interested in licensing the technology for further research and development.