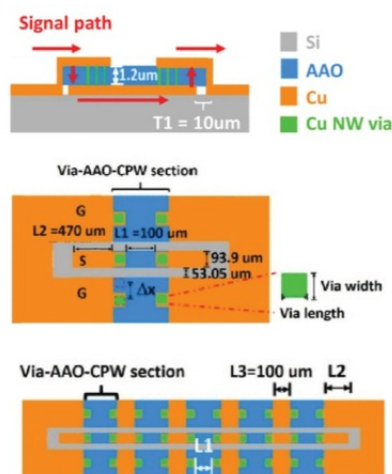




Design of ultrathin nanowire-based integrated via for CMOS application in millimeter-wave frequencies

A device for millimeter-wave frequency CMOS applications with decreased loss made with bundles of integrated nanowires.



Technology ID

2021-161

Category

All Technologies

Engineering & Physical

Sciences/Nanotechnology

Engineering & Physical

Sciences/Processes

Engineering & Physical

Sciences/Semiconductor

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IP Status: US Patent Issued; Patent No. 12,142,805

Applications

- High-Frequency 3D Integrated Circuits
- Millimeter-Wave Communications
- Submillimeter-Wave Communications

Technology Overview

Future millimeter- and submillimeter-wave communication systems are the key enablers to Internet of Things technology, autonomous vehicles, and low-power cube-satellites, however, at these high frequencies, loss from vias becomes prohibitive. Researchers at the University of Minnesota have developed a device integrating bundles of nanowires in an integrated via structure to decrease power loss. This device utilizes the decreased via thickness (1.2 μm vs 50-250 μm) to reduce insertion loss of a test line with two G-S-G vias at 40 GHz from 0.21-0.93 dB down to 0.095 dB.

Phase of Development

TRL: 3-4

Working prototypes have been developed.

Desired Partnerships

This technology is now available for:

- License
- Sponsored research
- Co-development

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Press Releases

[University of Minnesota College of Science & Engineering](#) January 29, 2021

Researchers

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References

1. Y. Zhang, J. Um, B. Stadler, R. Henderson and R. Franklin(2021) ,
<https://ieeexplore.ieee.org/document/9369363>, IEEE Microwave and Wireless Components Letters, 31, 693-696