



Computational Random Access Memory (20130219, Dr. Jian-Ping Wang)

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RAM with Logic Circuits

Computational-RAM (CRAM) technology featuring a low-power, non-volatile processor architecture produces very high computational performance. The technology conserves power by integrating computational elements into memory arrays so that data no longer needs to move to a separate location for processing. Since data does not have to be accessed sequentially through the interconnect network, multiple independent computations can be performed simultaneously. By using non-volatile magnetic memory cells (e.g., magnetic tunneling junctions (MTJ)) data stored in the memory cells is not lost due to temporary interruption in the power supply—or even if the power supply is entirely switched off. Lack of charge leakage implies that data persists in the memory for longer duration without power. This paradigm also reduces current leakage in memory cells and avoids associated power inefficiency and speed constraints, and its small size and regular memory cell structure accommodates larger memory sizes within the same area.

Technology ID

20130219

Category

Engineering & Physical
Sciences/Semiconductor

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Smaller Size, Lower Power Requirements

Conventional processor architectures use separate elements for data storage and computation, with a separate logic unit connected via interconnects to memory. To perform a computation, data must be fetched from memory, operated on and then stored back to memory. The interconnect between data storage and computation can bottleneck these architectures and consume more than 80% of total processor power, while scaling transistor features to smaller sizes results in current leakage and power consumption that severely limit performance. This CRAM architecture creates logic circuits in semiconductor chips with built-in memory that is particularly dense and low power, which addresses the expected scaling limits with current CMOS technologies. In addition, using logic with built-in memory eliminates interconnect power

loss. While others have demonstrated single devices based on this paradigm, those devices often require complicated CMOS circuitry that negate any advantages or do not provide random access, (i.e. ability to arbitrarily manipulate variables). The architecture and associated method for executing computations suggests significant savings in area and power over contemporary architectures.

BENEFITS AND FEATURES:

- MTJ based CRAM processor provides better performance
- MRAM (magnetic random access memory) based CRAM architecture based on a memory layout likely high density
- Non-volatile memory cells in general (e.g., Magnetic Tunneling Junctions (MTJs), or any resistance memory cell (R-RAM), etc.)
- Very high computational performance
- Faster and more power efficient
- Data not lost due to interruption in the power supply
- Reduces current leakage in memory cells

APPLICATIONS:

- Ideal for massively parallel operations (e.g., HD video processing)
- Digital Video / Still Cameras / multi-spectral CCD sensors
- Streaming Processors / Networking Processors
- Projectors / Display Processors
- Medical Scanning / Imaging processors
- Mobile Phones / Cellular Base Stations
- FPGA Fabrics
- Memory Controllers
- Smart Cards
- Media Players
- Cognitive computing unit
- Neuron networks

Phase of Development - Concept

Researchers

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