



# A counter based in-situ non-linearity measurement circuit in analog-to-digital converters

**A novel light-weight measurement circuit to characterize non-linearity in analog-to-digital converters.**

**IP Status:** US Patent Issued, [10,951,221](#)

## Applications

- Analog-to-digital converters in communication systems, electronic instruments, testing equipment, sensors, embedded systems
- High resolution ADCs or studying subtle shifts in ADC performance

## Technology Overview

Characterizing analog-to-digital converters (ADCs) is a challenging task because the performance of an ADC is sensitive to the noise in the measurement setup. Among these metrics, differential non-linearity (DNL) and integral non-linearity (INL) are the standard linearity parameters which are obtained from a histogram of the ADC codes for a slow triangular input voltage signal. The frequency of the triangular signal during a non-linearity test should be low enough to avoid any settling time issues. In the ideal case, all ADC codes appear the same number of times during a non-linearity test. In reality, however, some codes may have a higher or lower count than the ideal count due to non-linearity in the circuit and/or due to noise effects. This is because the input-output (IO) signals are switching at a high frequency while the ADC is performing the sensitive analog to digital conversion. Consequently, this setup is not suitable for characterizing high resolution ADCs or studying subtle shifts in ADC performance.

Researchers at the University of Minnesota have developed a novel light-weight measurement circuit employing a bank of counters for precise differential non-linearity (DNL) and integral non-linearity (INL) characterization. This technology is immune to measurement noise as the ADC operation and data transfer operation are separated in time. Compared to the setup in previous inventions, this design is simpler and more compact as only the count values are stored on-chip.

## Phase of Development

**TRL: 4x**

Working prototype - results from an integrated circuit chip in 65nm technology is obtained.

## Desired Partnerships

This technology is now available for:

- License
- Sponsored research
- Co-development

## Technology ID

2019-142

## Category

Engineering & Physical Sciences/Design Specifications  
Engineering & Physical Sciences/Instrumentation, Sensors & Controls  
Engineering & Physical Sciences/Semiconductor

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## Researchers

- [Hyung-il \(Chris\) Kim, PhD](#), Professor, Electrical and Computer Engineering

## References

1. Park, Gyusung, Minsu Kim, Nakul Pande, Po-Wei Chiu, Jeehwan Song, and Chris H. Kim , [https://ieeexplore.ieee.org/abstract/document/8780279?casa\\_token=bkjeevp38E0AAAAA:CcLk\\_\\_qutjyS7CsHnESmnmUe0qPgChnc52vNbjQwR82dvz-IBJ-zbjFeH-4OaylHF7sa5UE](https://ieeexplore.ieee.org/abstract/document/8780279?casa_token=bkjeevp38E0AAAAA:CcLk__qutjyS7CsHnESmnmUe0qPgChnc52vNbjQwR82dvz-IBJ-zbjFeH-4OaylHF7sa5UE), In 2019 IEEE Custom Integrated Circuits Conference (CICC), pp. 1-4. IEEE, 2019.