



Ultra-low Power Carbon Nanotube Logic Circuits (20140082, Dr. Chris Hyungil Kim)

Technology No. 20140082

Thin Film Transistors with Semiconducting Carbon Nanotubes

This technology, co-owned with Northwestern University, uses thin-film transistors that employ sorted semiconducting carbon nanotubes and local metal gate structures to tune the threshold voltages of both p-type and n-type devices to enable ultralow power CMOS logic. Furthermore, their input and output voltages are suitable for logic gate cascading, making these circuits ideal for large-scale integrated circuits. The digital logic circuits use p-type and n-type carbon nanotube based transistors which have tuned threshold voltages that enable ultralow power operation. This alignment is accomplished by incorporating local metal gate structures and sorted semiconducting carbon nanotubes. The resulting thin-film transistors are then integrated into three basic logic circuits: inverters, NOR gates, and NAND gates. These circuits display ideal input and output voltage behavior while maintaining subnanowatt power consumption.

Carbon Nanotube Logic Circuits Alternative to Silicon

Carbon nanotube logic circuits represent an alternative material to silicon (Si) for large area solution processed flexible electronic devices and offer additional benefits of mechanical flexibility and solution processability. Complementary metal-oxide-semiconductor (CMOS) logic circuits are the basis for all modern digital electronics, and commercial electronics are dominated by silicon CMOS technology. This technology offers high mechanical flexibility relative to conventional Si wafer based electronics, and because it is not limited to the size of a wafer, it is readily scalable to large area devices/applications and holds potential for low cost solution processing of active materials. Threshold voltage of p-type and n-type carbon nanotube transistors can be tuned systematically, and the technology enables complementary carbon nanotube transistors with better matching properties, significantly reducing static power consumption compared to existing technologies.

BENEFITS AND FEATURES:

- High mechanical flexibility relative to conventional Si wafer-based electronics
- Low cost solution processing of active materials
- Not limited to wafer size; scalable to large area devices and applications
- Ultra-low power consumption
- Exceptional noise immunity

APPLICATIONS:

- Digital Electronics
- Integrated circuit applications (e.g., microprocessors and memory, displays, large-area sensor arrays for environmental or biomedical sensing)

Phase of Development - Proof of Concept

Researchers

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Publications

[Subnanowatt Carbon Nanotube Complementary Logic Enabled by Threshold Voltage Control](#)

Nano Letters, 2013, 13 (10), pp 4810–4814; September 10, 2013

External Links

[VLSI Research Group](#)

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