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Design of Energy Efficient Microprocessor

Technology No. 20170334

IP Status: US Patent Issued # 10,866,630

Reduces processor voltage without reducing frequency

This technology is a new method that exploits dynamic timing slack (DTS) to reduce the voltage of a processor, based on the application being executed, without reducing the frequency. It automatically identifies DTS by analyzing an application binary and processor to determine parts of a design guaranteed not to be exercised by the application. The process then analyzes the timing safety of the constrained design at different voltages to determine the minimum safe operating voltage for an application/processor pair. Because a given application may not exercise the most timing critical paths of a processor, this process reduces voltage as long as all paths exercisable by the application meet timing constraints.

Enhances battery life of simple devices

Processors that run simple applications (e.g., for door/window sensors, remote sensors, IoT devices, heart rate monitors, etc.) require extended battery life. Demand for simple processors that are smaller and consume less power is growing as demand for the devices and sensors grows. Current techniques for optimizing processor design suffer performance and design time overheads. This new automated solution analyzes the software and the chip’s CAD file to identify portions of the processors that can be turned off or removed, thus enhancing the battery life of these simple devices.

Phase of Development

- Prototype developed.

Benefits

- Reduces power consumption of existing chips
- Enhances battery life of simple devices

Features

- Analyzes application binary and processor
- Determines microprocessor elements that cannot be exercised
- Analyzes timing safety of constrained design at different voltages
- Determines minimum safe operating voltage for an application/processor pair

Applications

- Chip / processor design
- Processor design/CAD software
- Tools for processor performance
- Internet of Things (IoT)
- Processor optimization

Researchers

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Publications

Exploiting dynamic timing slack for energy efficiency in ultra-low-power embedded systems
2016 ACM/IEEE 43rd Annual International Symposium on Computer Architecture (ISCA), Volume 44 Issue 3, June 2016, Pages 671-681

Interested in Licensing?

The University relies on industry partners to further develop and ultimately commercialize this technology. The license is for the sale, manufacture or use of products claimed by the patents. Please contact us to share your business needs and licensing and technical interests in this technology.