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Characterizing Soft-Errors in Advanced CMOS

Technology No. 20160069

Increases Sensitivity Towards Soft Errors

A novel back-sampling circuit increases target chain sensitivity towards soft errors without compromising measurement accuracy. Current technologies suffer from low sensitivity (most strikes go undetected) or large distortion (pulse width information is inaccurate). The new circuit has skew in the direction that favors lowering the switching threshold, which in turn enhances the sensitivity of the circuit to radiation strikes and results in pulse expansion instead of contraction. These methods measure accurate pulse width, lower the switching threshold, and use current starved inverters to control the bias conditions, thereby determining amplitude information as well as the pulse width.

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Measures Pulse Width and Amplitude, Improves Sensitivity

Assessing circuit design and semiconductor design sensitivity is critical for rapidly evolving new technologies, but current development tools lack the capability for increasing sensitivity of pulse detection circuits. One solution is lowering the supply voltage, but that can introduce inaccuracies in the local-sampling flops and increase susceptibility to strike. Another limiting factor in electronic circuit performance is clock jitter, the deviation from the true periodicity relative to a reference clock source. While phase-locked loop (PLLs) control systems track the timing of an input source and adjust the corresponding oscillator in a feedback loop, their performance is ultimately limited by achievable resolution in input pulse measurements. These drawbacks are addressed by this new circuit technology, which provides time amplification for measuring finer resolution for improved phase locking for any time-to-digital (TDCs) of which PLLs are one type. Furthermore, the new approach starves the current path to each individual logic gate, improving sensitivity tenfold while directly sampling the pulse width information using a back-sampling chain interwoven with the main logic chain. The current starved inverter circuit provides flexibility in controlling bias voltages that can be used to control and change the skew, and hence sensitivity, of the chain.

BENEFITS AND FEATURES:

- Minimizes radiation-induced effects on electronic devices and systems
- 10x improvement in sensitivity
- May provide higher clock speeds
- May provide reduced power for a given clock speed

APPLICATIONS:

- Electronic circuits, components and devices
- Applications where pulse expansion is required
- Developing soft error predictor or simulator circuits with on-chip error monitoring
- Characterizing process variations in different CMOS process technologies

Phase of Development - Proof of concept complete. Initial testing successfully completed in an alpha particle accelerator facility.

Researchers

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